From pixels in ALICE and NA60 to their application in the PHENIX VTX upgrade

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I will briefly review:

- Why CERN pixel detector technology found our interest.
- Experience we have gained, and progress made in two years of work at CERN: NA60 experiment, ALICE-RIKEN collaboration.

And then focus on:

 Progress on a detailed breakdown of the PHENIX pixel assembly schedule, for the submission of the VTX Proposal.



Motivation

The ALICE Silicon Pixel Detector is very similar both in purpose and layout to the planned VTX Upgrade of PHENIX. Advanced, existing technology:

- CERN pixel detectors have a > 10 years R&D history and a list of successful applications: RD19 → Wa97, NA57, DELPHI
- Latest development for application in: ALICE, LHCb, NA60.
- → Aim at a cooperation with ALICE at CERN to profit as much as possible from those developments for a PHENIX application.





ALICE Pixel Detector:

Two barrel layers: $R_i = 39$, $R_0 = 76$ mm

Inner layer: $|\eta| < 1.95$

Total Si area: 0.24 m²

120 modules with 2 hybrid "ladders"; 5 pixel chips per ladder; bus, controller & link chips

Thickness: 350 µm Si

Pixels/chip: 8192

Pixel size: 50 x 425 µm²

Sec. vertexing (c,b) in central Pb-Pb collisions. Track impact parameter resolution: < 50 μm $(p_{T} > 1.3 \text{ GeV/c}).$



Strategy

Start collaboration at CERN, work there and obtain experience with this technology.

1) Since December, 2001: participation from RIKEN and Stony Brook in the

NA60 experiment

Dimuon spectrometer of CERN heavy ion programme (NA10/38/50), completed with a pixel vertex spectrometer that is based on pixel detector technology developed at CERN for and by the ALICE experiment.

2 RIKEN persons involved full-time. Participated actively in design, production, commissioning, and operation of the pixel detectors in the NA60 experiment.

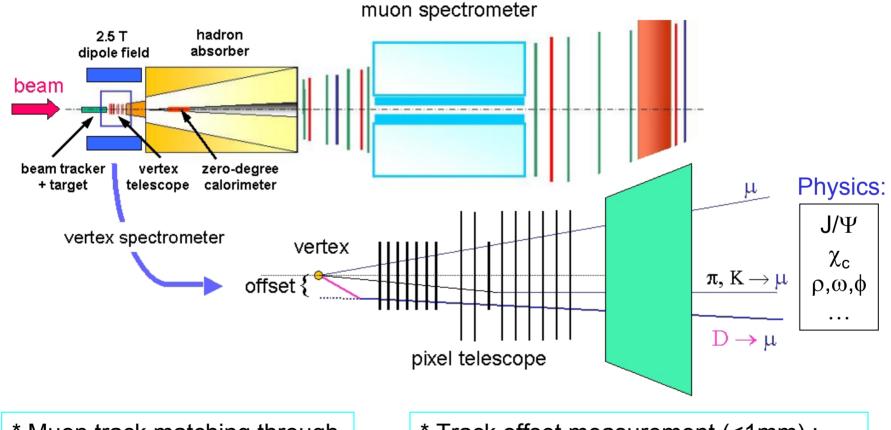
2) Memorandum of understanding between RIKEN and ALICE collaboration was established, for a participation in the ALICE Pixel Detector project.

Covers: joined production of detectors, associated development of front-end electronics, output of pixel detector modules for PHENIX.

Effective since Summer, 2003. Several RIKEN persons working as associated collaborators with the ALICE pixel group.



The NA60 Experiment: Study of Prompt Dimuon and Charm Production with Proton and Heavy Ion Beams at the CERN SPS

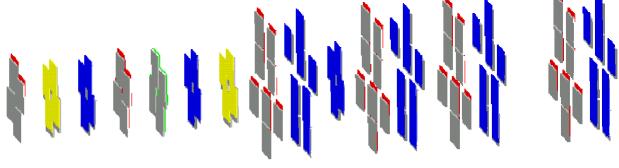


* Muon track matching through the hadron absorber.

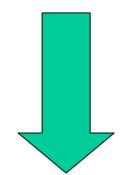
* Track offset measurement (<1mm): Separate **charm** from **prompt** dimuons

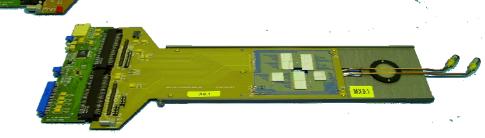


NA60 silicon pixel telescope



- 11 tracking points with good acceptance
 - 8 "small" 4-chip planes, plus
 - 8 "big" 8-chip plane
- ~ 3% X₀ per plane
 - 750 µm Si read-out chip (not thinned)
 - 300 μm Si sensor (moderate thickness)
 - ceramic hybrid: carries readout bus, mech. support
- 800'000 channels telescope
 - 96 ALICE1LHCb single-chip "assemblies"
 - ALICE pilot chip V1
 - CERN GOL chip
 - NA60 specific power supply, cooling scheme, PCI communication and readout system.



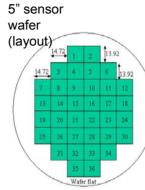




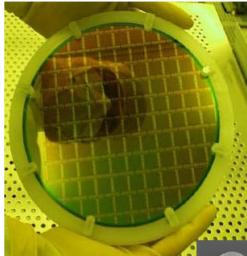
Design, Prototyping, Assembly



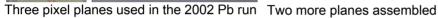


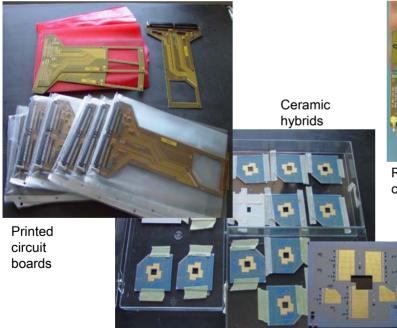


8" ALICE1/LHCb chip wafer prepared for bump-bonding to yield the pixel detectors



20 µm solder bump bond (VTT, Finland)



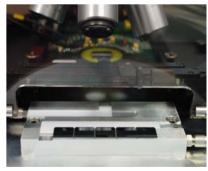




Readout electronics: ALICE pilot chip, GOL, interface to NA60 PCI

Cooling structure on a module

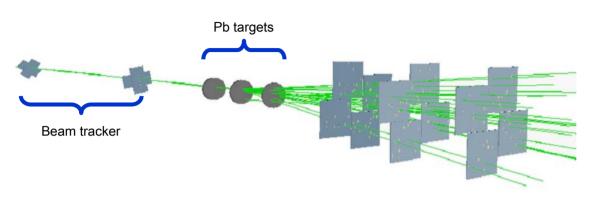




Quality check: Pixel detector assemblies on probe station

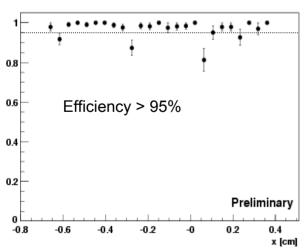


Three pixel planes, test in summer 2002

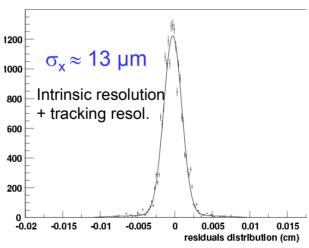


- 20 and 30 GeV/c Pb ions
- 3 Pb targets: 1.5, 1.0, 0.5 mm thick
- Three 4-chip modules
- Threshold: 2000 e
- Noisy pixels << 0.5%

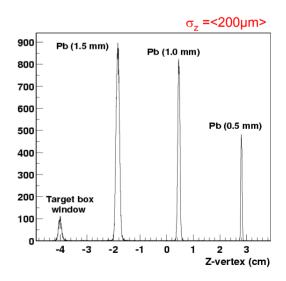
Detector efficiency:



Spatial resolution:

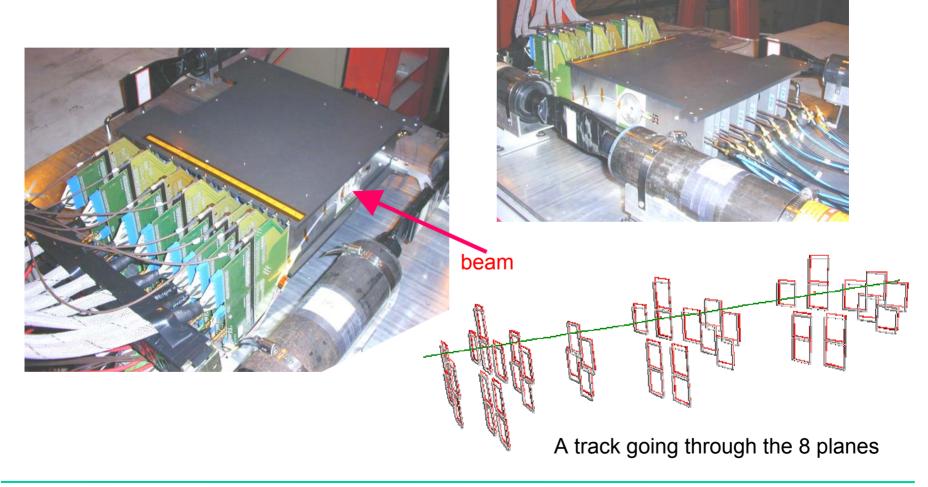


Vertex measurement:



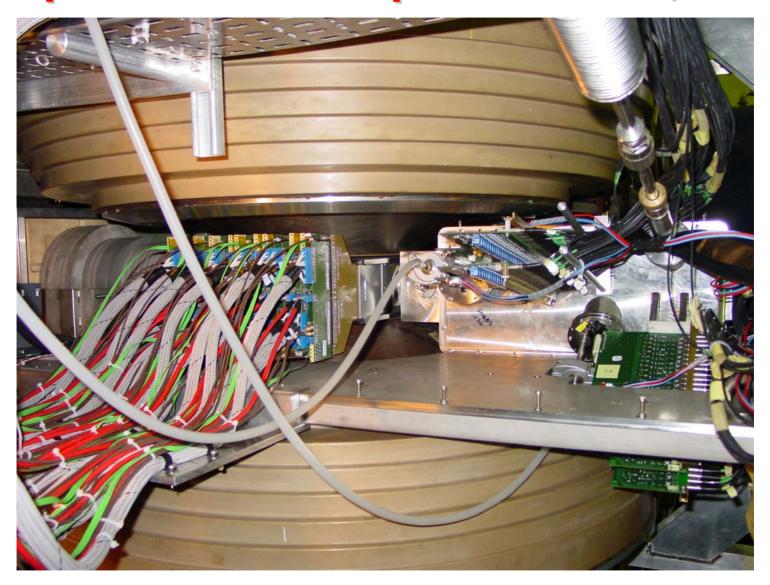


Test beam of ½ of the pixel telescope, summer 2003





Completed Vertex Spectrometer, 9/2003

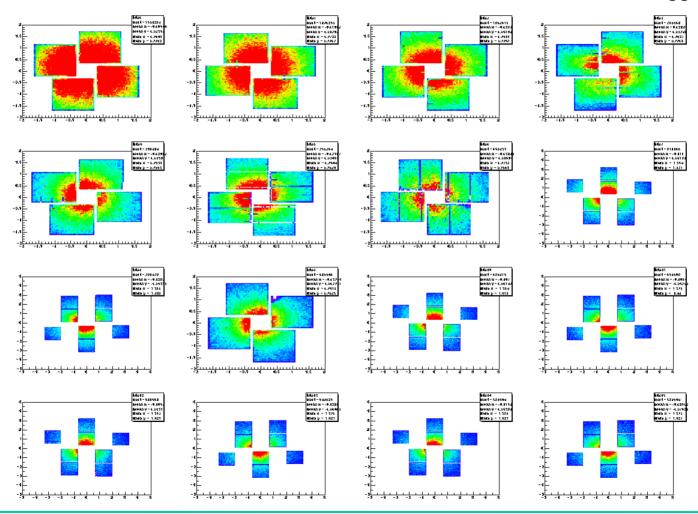




Online monitoring, In-In run, Fall 2003

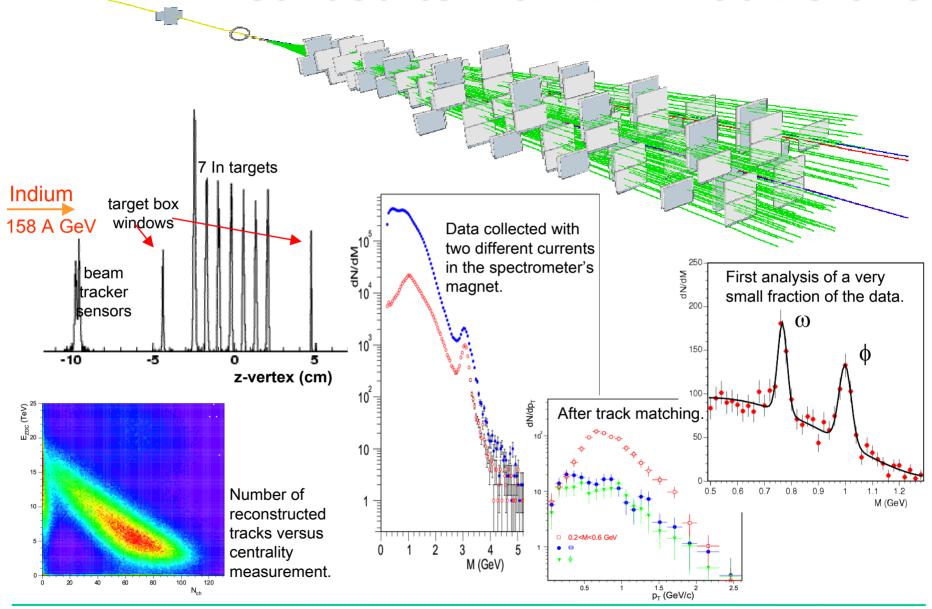
All modules worked fine!

NA60 collected data from several hundred million dimuon and min. bias triggers.





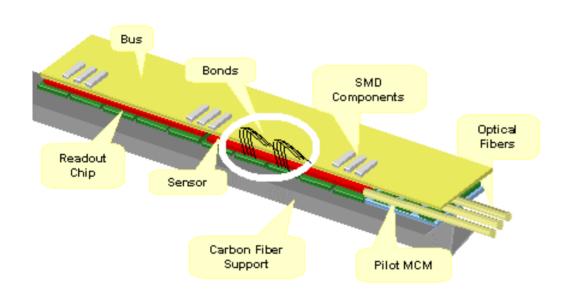
First results from In-In collisions



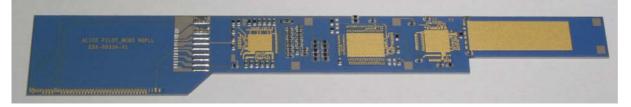


ALICE Silicon Pixel Detecor

The project is in an advanced state. The components of the pixel ladder are all developed. Production and assembly details are being finalized.



Pilot module: Analog Digital GOL Optical Pilot Pilot Diodes

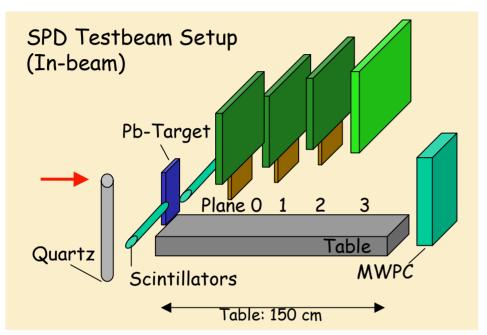


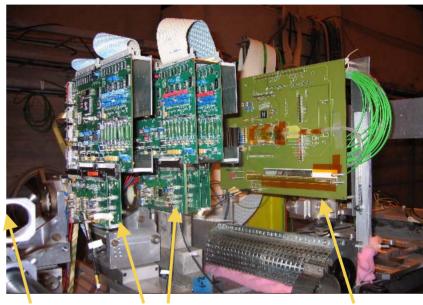
- Pixel readout chips: OK.
- Sensors: choice of passivation material not yet decided.
- Bump bonding:
 Resumed at VTT for ALICE after exclusive production period for NA60 in 2003.

 Test production ongoing.
 Good ladders were produced.
- Bus: first Al-Kapton production has been delivered.
- Pilot module: all chips are final by now. Board produced.
- Readout system: tested with all final components, in lab and test beam.
- Mechanical assembly: procedure and tools ready.



ALICE pixel test beam, Fall 2003 at SPS





Single-Chip Assemblies

- characterization of a detector ladder.
- test of full readout chain, including prototype bus and full pilot module connected to pixel bus.

Target

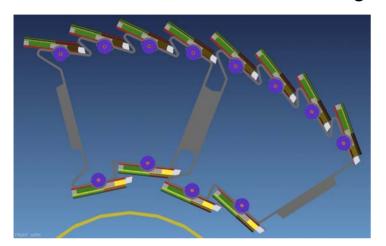
- RIKEN participation in the test beam effort.

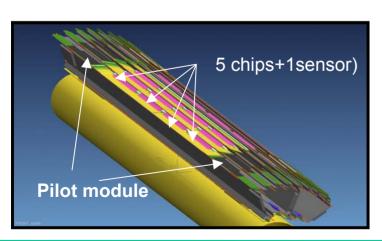


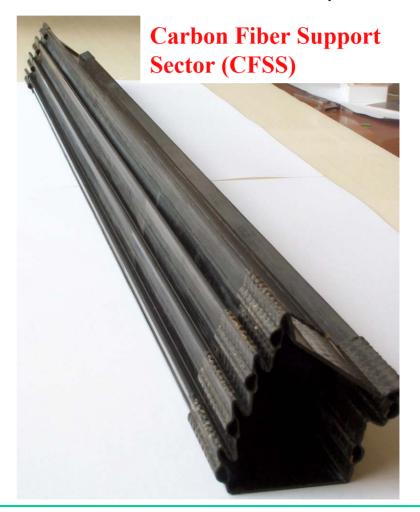
Ladder

ALICE Goal for 2004:

- (Part of) a sector equipped with pixel detector modules.
- System test in lab and test beam, together with other Inner Tracker components.









Production of ladders for PHENIX bump bonding-

Bump bonding for PHENIX ladder production will take place as part of the ALICE ladder production, within the ALICE time slots at VTT.

Tentative schedule (to be finalized by ALICE-VTT in February):

Year 2004

From Feb-2 to Feb-16

From Feb-16 to April (Mid) production of PHENIX Sensor wafers

From April (End) to May(Mid)

From July(Mid) to Nov

design of PHENIX Pixel Sensor

Assembly production at VTT(I)

Assembly production at VTT(II)

>> now <<

aim at production of first PHFNIX ladders

Year 2005

From Jan to March Assembly production at VTT(III)

From April to May Assembly production at VTT(IV)

From July to August Assembly production at VTT(V)



Production of ladders for PHENIX - readout chip test -

- 16 wafers with 86 chips each are available at CERN for RIKEN.
 More than enough for PHENIX project.
- We have experience on wafer and ladder testing (from ALICE/NA60 work).
 - CERN-EP probe station fully set up: it is reserved for ALICE/LHCb work.
 - RIKEN-owned wafer probe station will be available at CERN from early March, 2004:
 - → exclusively for PHENIX work, important to decouple ALICE-PHENIX testing.
- · Setup of probe station in March.
- Goal: probe one PHENIX readout chip wafer in March-April
 - → chips for first ladder production.
 - → expectation: at least 50% wafer yield, i.e. at least ~40 ALICE1LHCb chips, good for some first 5-10 4-chip ladders.
- Probe station will later be used for the ladder tests during "mass production".
 See schedule.

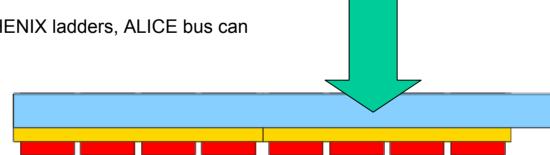


Production of ladders for PHENIX - pixel bus -

- Biggest issue of the project.
- challenge: in order to reach a 4-times faster ladder readout time as in ALICE architecture. the bus has to be parallelized: Parallel branches of the readout bus, higher density of readout lines.

Non-trivial in Aluminum-Kapton material, even in ALICE architecture.

- No industrial vendor in Europe was capable to build the ALICE bus.
- At CERN EST-DEM workshop, the production of the ALICE pixel bus has been successful.
- R&D study is carried out in Japan.
- Capabilities of industry in US to be researched as well.
- For testing purpose of PHENIX ladders, ALICE bus can be used initially.





Production of ladders for PHENIX - PHENIX pilot chip, pilot module -

- Second-biggest issue of the project.
- Perform parallel readout of the front-end chips, to arrive at 200 μ s \rightarrow 50 μ s readout time.
- Pilot module design depends on how the pilot chips will look like (size), and on the available space around the VTX detector.
- Two approaches on the pilot chip:

CERN/RIKEN: New design in 0.25 µm CMOS, with all functionality of the ALICE design, plus:

Initially 50% reduced readout time: read two chips in parallel: $2 \rightarrow 1$

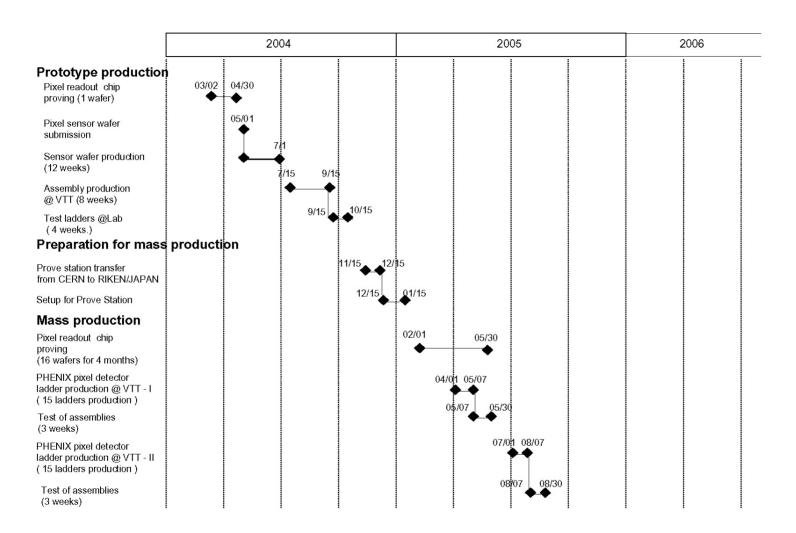
Aim at finished design for the next multi-wafer-project submission at CERN (around middle of May -June 2004, then November-December).

ISU: $4 \rightarrow 1$ design in radhard FPGA technology has been made.

• Discussion on merged effort, to meet first submission deadline at CERN.



PHENIX pixel schedule 2004-2005





PHENIX pixel schedule 2004-2005

